An Integrated Four-Phase Buck Converter Delivering 1A/mm^2 with 700ps Controller Delay and Network-on-Chip Load in 45-nm SOI

N. Sturcken, M. Petracca, S. Warren, L. P. Carloni, A. V. Peterchev*, and K. L. Shepard

Columbia University
500 West 120th Street
New York, NY 10027

*Duke University
2212 Trent Drive
Durham, NC 27710

***Abstract*- We present a four-phase integrated buck converter in 45nm SOI technology. The controller uses unlatched pulse-width modulation (PWM) with nonlinear gain to provide both stable small-signal dynamics and fast response (~700ps) to large input and output transients. This fast control approach reduces the required output capacitance by 5X in comparison to a controller with latched PWM at similar operating point. The converter switches at 80MHz and delivers 1A/mm^2 at 83% efficiency and 0.66 conversion ratio.**

I. Introduction

Performance-per-watt is an increasingly important metric for microprocessors as it is now common for the thermal envelope to limit computational performance of an IC. Dynamic voltage and frequency scaling (DVFS) can improve performance-per-watt by reducing wasted power when logic is idling or performing a low priority task [1]. The benefits of DVFS are best realized when implemented with high granularity of voltage and frequency domains, for example, individually optimizing the power consumption of each core in a many-core processor according to workload. Unfortunately, conventional switched–inductor board level voltage regulator modules (VRMs) are poorly suited for such a granular implementation because of the need to distribute many supplies from board to chip. Integrated DC-DC power converters offer the scalability required while allowing power to be brought on-die at higher voltage, reducing current levels, associated power network impedance requirements, and I^2R losses.

Recent work has explored integrated voltage regulators (IVRs), including both switched-capacitor and switched-inductor IVRs. Switched-capacitor converters have shown high efficiency at reasonable current densities but have done so only at fixed conversion ratio and without addressing transient requirements [2, 3]. Meanwhile, switched-inductor (buck) converters have shown high current densities and efficiencies with a continuous range of conversion ratios, making buck converters the most promising of IVR candidates [4-7].

Transient requirements pose a major challenge in development of IVRs as microprocessors require tight voltage regulation even during large load-current steps. Some early switched-inductor IVRs addressed transient requirements by employing a multi-phase hysteretic controller that minimizes delay, providing an almost instantaneous response to transients [4, 5]. Unfortunately, the closed loop behavior is especially difficult to predict for these nonlinear controllers and the loose synchronization of phases produces an under-damped large-signal response as evident in time-domain waveforms. Subsequent works [6, 7] use more traditional, pulse-width modulation (PWM) controllers and rely on an abundance of package-level decoupling capacitance to compensate for increased controller delay. The primary drawback to this approach is the dependence on package-level capacitance, which will be unavailable with higher levels of integration. In contrast, the four-phase buck converter presented here, fabricated and tested in 45-nm SOI, employs an unlatched PWM modulator and nonlinear feedback to concurrently provide PWM-like synchronization of multiple phases, linear small-signal dynamics (ensuring stability and load-line regulation), and nearly instantaneous response to large-signal input and load-current transients without the need for large output decoupling.

II. Critical Output Capacitance

Table 1 summarizes key parameters for the proposed IVR. For these parameters, we will determine the constraint on minimum output capacitance (C_{OUT}) in an effort to reduce this capacitance and improve current density.

Assuming availability of integrated capacitors with fast ESR time constants ($\tau_C=r_C C$), the optimal load-transient response is achieved when the output voltage (v_{OUT}) follows a dynamic load-line [8]

$$V_{OUT} \rightarrow v_{REF,DC} - R_{OUT}\frac{1+s\tau_C}{1+sR_{OUT}C_{OUT}} \times i_{LOAD} \quad (1)$$

R_{OUT} is the desired DC output resistance, commonly set to

$$R_{OUT} \rightarrow \frac{2 \times \Delta V_{OUT}}{\Delta I_{LOAD}} \quad (2)$$

To avoid chaotic behavior, the crossover frequency for the loop gain, f_C, should be set according to the switching stability guideline [8]

$$f_C \leq \frac{N \times f_{SW}}{6} \quad (3)$$

TABLE I
Proposed IVR Specifications

V_{IN}	input voltage	1.5V
$I_{LOAD,MAX}$	max. load current	1.2A
ΔI_{LOAD}	max. dynamic load step	600mA
τ_I	load step time constant	100ps
ΔV_{OUT}	output tolerance band	±30mV
ΔV_{OS}	Max. transient overshoot	40mV
R_{OUT}	closed loop output resistance	100mΩ
f_{SW}	switching frequency	80MHz
N	number of phases	4
L	inductance per phase	26nH

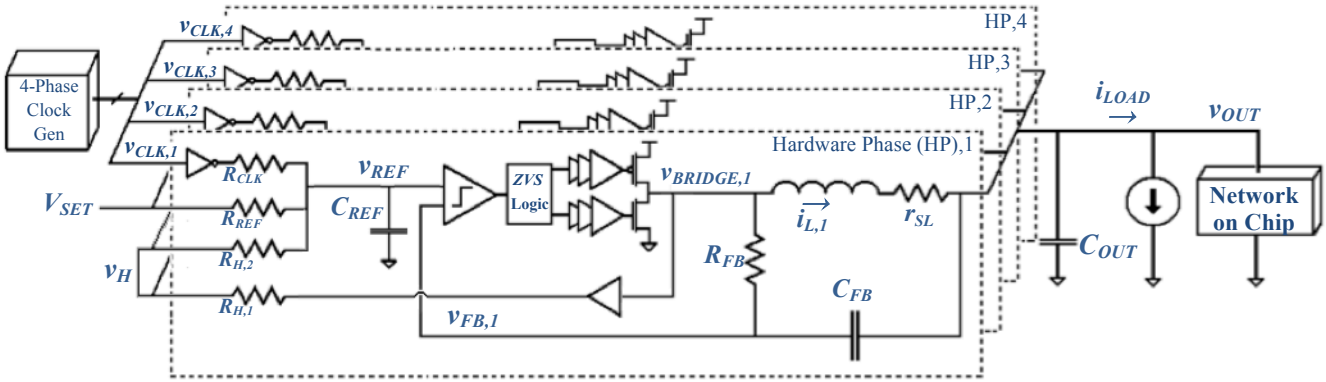

Fig.1: System level diagram of integrated power chip including NoC load

In order to achieve dynamic load line regulation, the output capacitor pole must be placed within f_C, this determines the constraint on minimum C_{OUT},

$$C_{OUT} \geq \frac{1}{2\pi R_{OUT} f_C} \tag{4}$$

Unfortunately, this value of C_{OUT} may not be sufficient in the presence of large load-current steps, which can lead to duty cycle saturation in the controller response, limiting the feedback gain and subsequently causing significant deviation from the load-line (overshoot). The critical capacitance, C_{CRIT}, is the approximate minimum C_{OUT} that limits output voltage overshoot to the tolerance specified in Table 1, ΔV_{OS}, during a worst-case load transient. C_{CRIT} is derived in [8] as

$$C_{CRIT} = \left(\frac{t_L}{2} + \frac{\tau_C^2}{2t_L} + t_d - \tau_1\right) \Big/ \left(R_{OUT} + \Delta V_{OS}/\Delta I_{LOAD}\right) \tag{5}$$

where $t_L = L\Delta I_{LOAD}/(N(V_{IN}\text{-}v_{REF,DC}))$ and t_d is the delay time for the controller to saturate the duty cycle. Small τ_C and t_L can be obtained with integrated capacitors and multiple phases respectively, in which case t_d tends to dominate the numerator of (5). In Section III, we describe a controller design with near immediate response to large load steps (fast t_d) that allows us to reduce C_{OUT} to less than 23nF for the specifications of Table 1.

III. Controller Design

Overview. Fig. 1 shows a system level diagram of the chip. A four-phase buck converter provides a regulated supply voltage to a digital load in the form of both a 64-tile network-on-chip (NoC) and a programmable current source capable of generating load-current steps of 1A with slew rates of ~1A/100ps. The converter occupies 0.75mm^2 including all input and output decoupling capacitance (0.32mm^2 excluding these capacitors). It operates with a switching frequency, f_{SW}, of 80MHz and voltage ripple of < 1mV. The down-converter supports a continuous range of conversion ratios from a 1.5V supply with a load current as high as 1.25A. The driver switches are thick-oxide floating body FETs where the widths have been optimized for 80MHz switching and 300mA per phase. A discretely programmable dead-time can be added to the nMOS turn-on transition, allowing zero voltage switching (ZVS) when v_{BRIDGE} transitions from high to low. Four 26nH, SMT-0402 air-core inductors are integrated on top of the chip by bond-wire connections. The inductance value is chosen to limit current ripple such that the converter efficiently operates in continuous conduction mode at f_{SW} of 80MHz and i_{LOAD} of 500mA. Use of the proposed control scheme allows us to reduce the total output capacitance, C_{OUT}, to ~23nF, including explicit MOS capacitors and non-switching gate capacitance from the digital load.

The buck converter is composed of four identical hardware phases (HP) and clock generation circuitry that provides the switching frequency and phase for each of the HPs, $v_{CLK,1\text{-}4}$. Within each HP, v_{CLK} is superimposed onto a DC reference voltage, V_{SET}, by means of R_{CLK} to create a triangle wave reference input to the controller, v_{REF}, that is centered at the desired DC output voltage, $v_{REF,DC}$, as shown in Fig. 2.

$$v_{REF,DC} = V_{SET}\frac{R_{CLK}}{R_{REF}+R_{CLK}} + \frac{V_{IN}}{2}\frac{R_{REF}}{R_{CLK}+R_{REF}} \tag{6}$$

The feedback voltage, v_{FB}, is a superposition of the bridge voltage, v_{BRIDGE}, at low frequencies and the output voltage, v_{OUT}, at high frequencies. The comparison of v_{REF} and v_{FB} at the delay-optimized continuous comparator determines the steady state duty-cycle, D, such that the DC values, $v_{REF,DC}$ and $v_{FB,DC}$, are equal. The DC output resistance, R_{OUT}, of the IVR can be tuned by $R_{H,1}$ and $R_{H,2}$ according the equation

$$R_{OUT} = r_{sl}' - r_{mos}'\frac{R_{H,1}+R_{H,2}}{R_{REF}\|R_{CLK}} \tag{7}$$

where r_{sl}' and r_{mos}' are the effective series resistance of the inductors and switches respectively.

Large-signal behavior. The time constant, $R_{FB}C_{FB}$, is designed to be ~30% longer than $R_{CLK}C_{REF}$ such that in steady state, v_{FB} will slew behind v_{REF} as shown in Fig. 2. In the event of a load current step, the resulting $\delta v_{OUT}/\delta t$ across

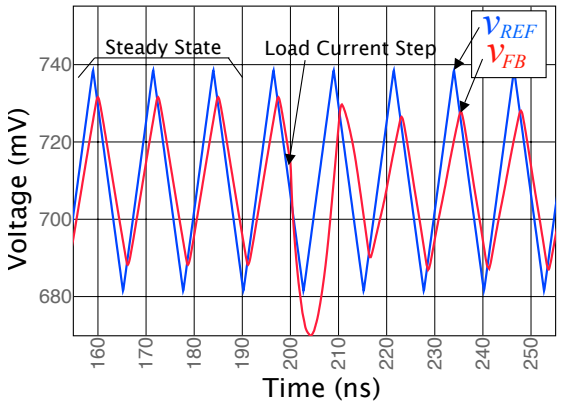

Fig.2: v_{REF} and v_{FB} during steady state and load transient, simulated

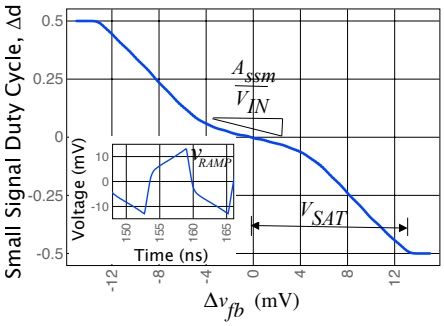

Fig.3: Δd as a function of v_{fb} perturbation amplitude, D=0.5

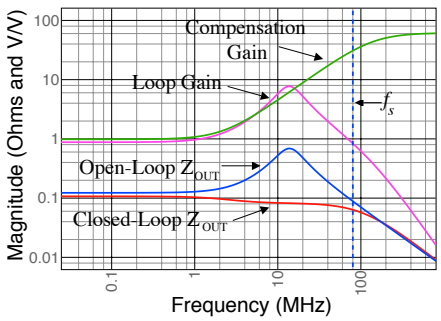

Fig.4: Small signal transfer functions and output impedance

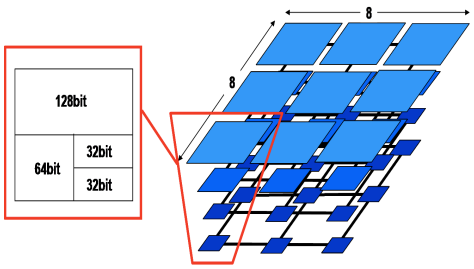

Fig.5: Network-on-Chop Organization

C_{OUT} couples through C_{FB}, and causes v_{FB} to cross v_{REF}. At this point, the comparators will switch state and the output drivers will apply the appropriate voltage at v_{BRIDGE}. Each of the HPs responds asynchronously, such that all of the inductors exert the maximum $\delta i/\delta t$ within a fraction of $1/f_{SW}$. When an HP becomes unsynchronized, the difference between v_{FB} and v_{REF} is larger and the HP's sensitivity to $\delta v_{OUT}/\delta t$ is reduced, driving the HP back to proper synchronization. In this manner, the controller simultaneously provides near immediate asynchronous response to load transients and strong synchronization between HPs in steady state.

The total controller delay during a worst case load transient is ~700ps according to simulation, 325ps for v_{FB} to cross v_{REF}, 160ps for the comparators to switch, and 200ps for the digital delay through ZVS logic and driver buffers. With this short delay time, C_{CRIT} required to meet the specifications in Table 1 is only 20nF according to (4).

Small signal dynamics. The small-signal dynamics can be determined using a combination of conventional linear circuit analysis and circuit averaging, if we assume that the frequency content of a small-signal perturbation, Δv_{FB}, is sufficiently below f_{SW} for averaging to be valid. The small-signal, steady state gain, A_{ssm}, of the comparator stage is similar to a conventional PWM modulator with the exception that both v_{REF} and v_{FB} have large signal components at f_{SW} (Fig. 2) in steady state and, hence, the effective PWM ramp signal is $v_{RAMP} = v_{REF} - v_{FB}$ as shown in Fig. 3 inset. A_{ssm} is inversely proportional to the slope of v_{RAMP} where it intersects Δv_{FB}. Fig. 3 shows the small signal change in the duty cycle, Δd, as a function of Δv_{FB}. When $|\Delta v_{FB}| < 4$mV the gain through the comparator is linear and approximated as

$$A_{SSM} \approx \frac{4 \times f_S}{\frac{1}{R_{CLK} C_{REF}} + \frac{1}{R_{FB} C_{FB}}} \qquad (7)$$

but for larger deviations, $|\Delta v_{FB}| > 4$mV, the gain through the comparator is non-linear and increasing, which provides improved transient response to large transients. The remainder of the loop transfer function can be determined with linear circuit analysis; the derived transfer functions and small-signal output impedance are shown in Fig 4. The loop gain predicts stable small-signal dynamics with a phase margin of 70°. In comparing the open-loop and closed-loop output impedance, we see that the controller successfully regulates to a dynamic load-line. The output capacitor ESR zero occurs above 100GHz, beyond the range of Fig. 4.

IV. Network On A Chip

A 64-tile network-on-chip (NoC) serves as a real digital load for the IVR. NoCs are becoming the basic interconnect infrastructure for complex systems-on-chip (SoCs). Since communication plays a key role in SoCs and given the very strict energy and performance requirements imposed on NoCs, recent designs have reserved a separate voltage-clock domain for the NoC alone [1].

Within our NoC each tile is composed of four cores to realize four independent 8x8 2D-mesh networks-on-chip NoCs (Fig. 5). Each individual NoC supports a different data parallelism, 128, 64, 32, and 32 bits, respectively. All NoCs adopt traditional wormhole flow-control and XY-dimension routing. The 2D-Mesh topology is achieved using 5x5 routers, where 4 I/O ports are attached to neighbor routers, and the fifth port is used for traffic injection/ejection. The traffic injected at each router is generated according to externally programmable parameters, such as packet length, inter-packet arrival and probability distribution of the destinations. Multiple parallel NoCs have been studied as power-efficient interconnect for supporting multi-class data traffic in complex SOCs [9].

IV. Experimental Results

The measured response to the worst-case load transient is shown in Fig. 6 with voltage overshoot of ~30mV. The output voltage, v_{OUT}, follows the load-line and closely matches simulated results with the exception of some ringing that occurs after the step.

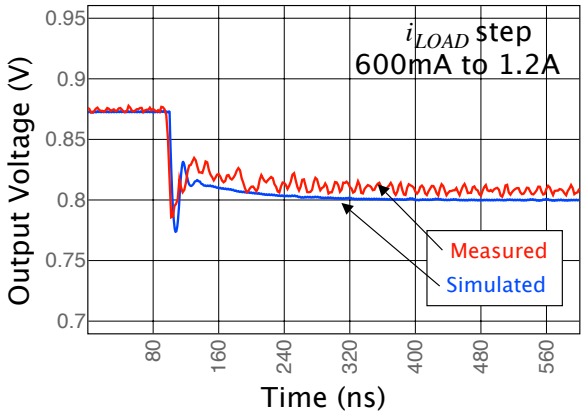

Fig.6: Load-current step response from proposed controller

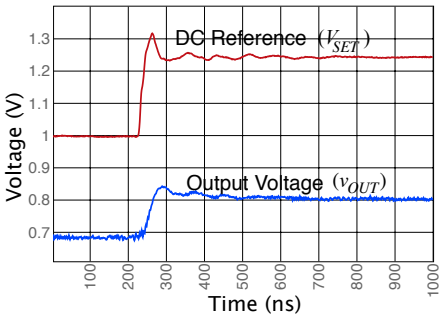

Fig.7: Measured input step response

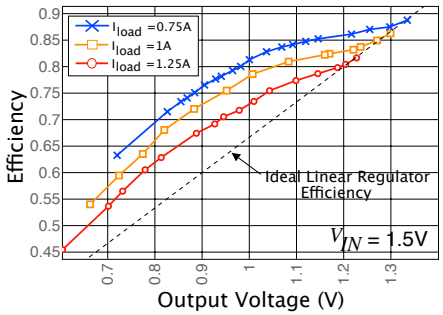

Fig.8: Measured converter efficiency

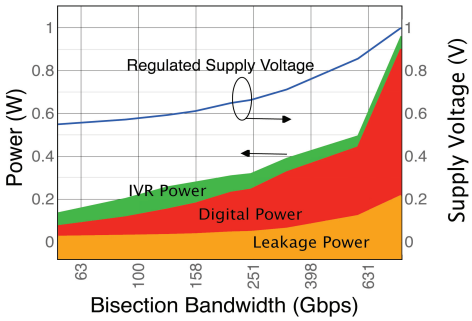

Fig.9: NoC power consumption with voltage and frequency scaling

We attribute this ringing to oscillation between C_{OUT} and the bondwire inductance on the ground return of the load. The estimated resonant frequency of this series LC, 75MHz, is the same as the frequency of ringing in Fig. 6. Fig. 7 shows the input step-up response, where we see a settling time for v_{OUT} of ~70ns.

Converter efficiency (Fig. 8) is hindered by the relatively high r_{SL}' of 120mΩ, which is dominated by bond wire resistance. An improved packaging strategy could substantially reduce r_{SL}'. The test chip achieves an efficiency of 83% at a current density of 1A/mm^2 (2.35A/mm^2 if decoupling capacitor area is not considered) and a 0.66 conversion ratio. Fig. 9 shows a breakdown of the NoC's power consumption with scaled voltage and frequency (bandwidth) that confirms the energy savings potential of DVFS. The chip is shown in Fig. 10 with dimensions of 3mm by 6mm.

Reduced decoupling requirement. We note again the required C_{OUT} of ~20nF to achieve these experimental result. For an IVR with the same power train and f_{SW} using a conventional feedback controller with latched PWM modulator, the required C_{OUT} would be > 100nF. Our controller design has improved the IVR's current density by roughly 2.2X.

V. Conclusions

We demonstrate a four-phase integrated buck converter with a fast controller that uses an unlatched PWM modulator and nonlinear feedback. The proposed controller provides predictable small-signal dynamics along with fast response to input and load-current steps, which facilitates a 2.2X improvement in current density. Combined with recent developments in inductive energy storage [10] a converter such as this will enable implementation of integrated power conversion on a large scale.

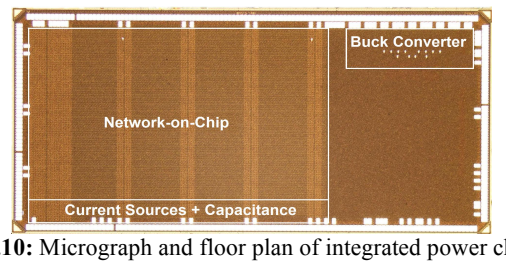

Fig.10: Micrograph and floor plan of integrated power chip

Acknowledgement

This work was partially supported by the U.S. Department of Energy, the National Science Foundation (Award #: 1018236), and the C2S2 and GSRC Focus Centers, two of five research centers funded under the Focus Center Research Program, a Semiconductor Research Corporation program

References

[1] J. Howard, *et al.*, "A 48-Core IA-32 Processor in 45 nm CMOS Using On-Die Message-Passing and DVFS for Performance and Power Scaling," *Solid-State Circuits, IEEE Journal of,* vol. 46, pp. 173 - 183, 2011.

[2] H. Le, *et al.*, "A 32nm fully integrated reconfigurable switched-capacitor DC-DC converter delivering 0.55W/mm2 at 81% efficiency," *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International,* pp. 210 - 211, 2010.

[3] L. Chang, *et al.*, "A fully-integrated switched-capacitor 2:1 voltage converter with regulation capability and 90% efficiency at 2.3A/mm2," *VLSI Circuits (VLSIC), 2010 IEEE Symposium on,* pp. 55 - 56, 2010.

[4] G. Schrom, *et al.*, "A 480-MHz, multi-phase interleaved buck DC-DC converter with hysteretic control," *2004 IEEE 35th Annual Power Electronics Specialists ...,* Jan 1 2004.

[5] P. Hazucha, *et al.*, "A 233-MHz 80%-87% efficient four-phase DC-DC converter utilizing air-core inductors on …," *IEEE Journal of Solid-State Circuits,* Jan 1 2005.

[6] G. Schrom, *et al.*, "A 100MHz Eight-Phase Buck Converter Delivering 12A in 25mm2 Using Air-Core Inductors," *Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE,* pp. 727 - 730, 2007.

[7] G. Schrom, *et al.*, "A 60MHz 50W Fine-Grain Package_Integrated VR Powering a CPU from 3.3V," *APEC - Special Presenation,* Feb 25 2010.

[8] A.V.Peterchev and S.R. Sanders "Load-Line Regulation With Estimated Load-Current Feedforward: Application to Microprocessor Voltage Regulators," *Power Electronics, IEEE Transactions on,* vol. 21, pp. 1704 - 1717, 2006.

[9] Y. J. Yoon, *et al.*, "Virtual channels vs. multiple physical networks: A comparative analysis," *Design Automation Conference (DAC), 2010 47th ACM/IEEE,* pp. 162 - 165, 2010.

[10] J. T. DiBene, *et al.*, "A 400 Amp fully Integrated Silicon Voltage Regulator with in-die magnetically coupled embedded inductors," *APEC,* vol. Special Presentation, Feb 25 2010.